

ENGINEERING TALENT FOR SEMICONDUCTOR INDUSTRY PROGRAM

ETS I

Introduction to Advanced Packaging Techniques: 2.5D, 3D, Chiplets and Integration Technologies



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INTRODUCTION

Step into the world beyond traditional scaling, where innovation is driven not just by silicon, but by how it is integrated. This course offers a compelling introduction to modern semiconductor packaging technologies—focusing on advanced packaging, heterogeneous integration, and chiplet architectures that power today’s High-Performance Computing (HPC) and AI systems.

COURSE OVERVIEW

Participants will gain clear insights into how cutting-edge packages are designed and manufactured, exploring key fabrication processes, system-level integration challenges, and reliability considerations. Through real-world industry case studies, the course connects theory to practice—revealing how leading semiconductor companies are pushing performance, bandwidth, and efficiency beyond conventional limits.

By the end of the course, participants will understand how advanced packaging is redefining system architecture and enabling the next generation of computing innovation.

COURSE OUTCOME

Upon successful completion this course, participants will be able to:

- Describe the fundamentals and evolution of semiconductor packaging technologies.
- Compare traditional and advanced IC packaging methods used in modern electronic systems.
- Explain the principles and processes of 2.5D/3D IC integration and heterogeneous packaging technologies.
- Identify key design, assembly, and reliability challenges in advanced semiconductor packaging.
- Evaluate advanced packaging solutions for applications in AI, HPC, mobile, and data center devices.

TARGET PARTICIPANT

This course is intended for technical professionals who wish to gain foundational knowledge and an introduction to Advanced Packaging.

- Managers
- Semiconductor Process Engineers
- Packaging Engineers
- Product & Test Engineers
- R&D Engineers in advanced packaging
- Q&R Engineers
- Design Engineers
- Yield Engineers
- Projects Leads
- Integration Engineers
- Technical professionals in the field of advanced packaging

Day	Training Outline
<p style="text-align: center;">Day 1 9am - 5pm (Module 1: Foundations & Overview of IC Packaging Techniques)</p>	<p>1. Fundamentals of Electronic Packaging</p> <ul style="list-style-type: none"> • Role and functions of semiconductor packaging • Evolution of packaging technologies from wire-bond to advanced packaging • Trends & Key Technologies • Introduction to 3D IC Packaging, 3D IC Integration and 3D Silicon Integration, Yield Introduction • Applications across mobile, High-Performance Computing (HPC), AI, and data center devices
	<p>2. Semiconductor Packaging Structures and Industry Trends</p> <ul style="list-style-type: none"> • Traditional vs advanced packaging architectures • Industry drivers: Moore’s Law limitations and system scaling • Emerging R&D trends in heterogeneous integratio
	<p>3. Overview of Advanced Packaging Technologies</p> <ul style="list-style-type: none"> • Flip-Chip packaging architecture and assembly • Wafer-Level Packaging (WLP) fundamentals • System-in-Package (SiP) integration approaches
	<p>4. Fan-In and Fan-Out Wafer-Level Packaging</p> <ul style="list-style-type: none"> • Fan-in Wafer-Level Packaging (WLP) architecture and limitations • Fan-out Wafer-Level Packaging (WLP) process flow and advantages • Panel-level packaging (PLP) developments • Industry case studies of fan-out integration
	<p>5. Workshop/Discussion</p> <ul style="list-style-type: none"> • Yield case study • Wire bond vs flip chip die area impact

Day	Training Outline
<p style="text-align: center;">Day 2 9am - 5pm (Module 2: 3D IC and Heterogeneous Integration)</p>	<p>1. Introduction to 3D IC Concepts and Heterogeneous Integration</p> <ul style="list-style-type: none"> • Evolution from traditional 2D packaging to 2.5D and 3D IC architectures • Definition and importance of heterogeneous integration in advanced semiconductor systems • Key advantages of 3D integration including higher bandwidth, reduced latency, and improved system performance • Industry applications in AI processors, high-performance computing, and mobile devices
	<p>2. Comparison of Fan-In vs Fan-Out Packages</p> <ul style="list-style-type: none"> • Overview of Wafer Level Packaging (WLP) technologies • Structure and characteristics of Fan-In Wafer Level Packaging (FIWLP) • Structure and advantages of Fan-Out Wafer Level Packaging (FOWLP) • Comparison of fan-in and fan-out packages in terms of I/O density, package size, and system applications
	<p>3. Overview of Chiplet Technologies, Standards and Design Consideration</p> <ul style="list-style-type: none"> • Introduction to chiplet-based architecture and system disaggregation • Overview of chiplet interconnect standards such as Universal Chiplet Interconnect Express (UCIe) and Advanced Interface Bus (AIB) • Key design considerations including bandwidth, latency, power delivery, and signal integrity • Benefits of chiplet integration including improved yield, modular
	<p>4. Interposer Technologies</p> <ul style="list-style-type: none"> • Silicon interposers • Organic interposers • Fabrication techniques and design considerations
	<p>5. Assembly Processes for 2.5D Integration</p> <ul style="list-style-type: none"> • Die-to-interposer bonding • Microbump assembly • Yield challenges in large interposer systems

Day	Training Outline
<p style="text-align: center;">Day 2 9am - 5pm (Module 2: 3D IC and Heterogeneous Integration)</p>	<p>6. Copper-to-Copper and Dielectric Hybrid Bonding</p> <ul style="list-style-type: none"> • Principles of copper-to-copper direct bonding technology • Overview of dielectric hybrid bonding mechanisms • Key process steps including surface preparation, alignment, bonding, and annealing • Advantages of hybrid bonding for fine pitch interconnect and high-density die stacking
	<p>7. Through Silicon Via (TSV) and Through Glass Via (TGV) Technologies</p> <ul style="list-style-type: none"> • Introduction to Through Silicon Via (TSV) technology for vertical integration • Key TSV fabrication steps including via etching, insulation, barrier deposition, and copper filling • Overview of Through Glass Via (TGV) technology and glass interposers • Comparison of TSV and TGV in terms of electrical performance, manufacturing complexity, and applications
	<p>8. Microbump Technology and Die Stacking Integration</p> <ul style="list-style-type: none"> • Introduction to microbump interconnect technology in advanced packaging • Microbump fabrication process including Under Bump Metallurgy (UBM) formation, bump deposition, and reflow • Role of microbumps in 2.5D interposer and 3D IC die stacking • Integration challenges including alignment accuracy, bump pitch scaling, and reliability
	<p>9. Case Study</p>

TRAINERS PROFILE



Ts Dr Norlin Nosbi serving as a lecturer and researcher at Mechanical Engineering Department, Universiti Teknologi Petronas (UTP) since 2018. She is a materials engineering specialist with over a decade of academic, research, and industry experience aligned with advanced materials applications. She holds a B.Eng. (Hons.), a MSc and a PhD in Materials Engineering from Universiti Sains Malaysia (USM), with a research focus on hybrid composites and 'synthesis, functionalisation and characterisation of carbon nanotubes/alumina hybrid compound and its nanocomposites in PDMS'. Her expertise spans nanomaterials, composite systems and surface engineering where the key domains supporting semiconductor packaging, reliability and failure analysis.

She contributes to teaching, research and consultancy in Materials and Mechanical Engineering, with emphasis on advanced materials, RF inductor material, coating and corrosion. Her academic experience is complemented by academic institute, training center and industrial exposure at USM, Advanced Technology Training Centre (ADTEC) and Lumileds (M) Sdn Bhd, where she was involved in composites technology instructor, research and teaching assistant positions and process development in composites and semiconductor manufacturing environments.

She has successfully secured and managed research funding approximately 0.56 million, demonstrating strong capability in leading high impact research projects. In addition, she has undertaken consultancy work valued 0.2 million, providing technical solutions and industry relevant insights. He also serves as a Co-Opted (Committee Member) for the Materials Engineering Technical Division (MaTD), in the Institute of Engineering Malaysia (IEM), contributing to professional development initiatives and technical advancement within the engineering community.

TRAINERS PROFILE



Dr. Nurul Azhani is a lecturer at Universiti Teknologi PETRONAS with over 8 years of academic experience in Materials Engineering, specialising in smart and functional materials. Holding a PhD from Malaysian-Japan International Institute of Technology (MJIIT), Universiti Teknologi Malaysia (UTM), including an international research attachment at Yamagata University.

Her research portfolio demonstrates strong leadership and sustained impact, having secured and managed research funding exceeding RM2 million, including more than RM400,000 as Principal Investigator. Her grants include national-level funding such as the Fundamental Research Grant Scheme (FRGS), international matching grants, and industry-funded projects in collaboration with Oil & Gas sector partners. This diverse funding background reflects her ability to translate academic expertise into impactful, application-driven research.

Her expertise centres on functional materials, material performance, and reliability in engineering systems. Through her participation in specialised trainings, collaborative research initiatives, and continuous engagement with semiconductor packaging developments, she is able to relate fundamental materials science concepts to key challenges in advanced packaging, including thermal management, interconnect reliability, and system integration.

Participants in her training programmes benefit from clear, structured explanations, relevant case-based discussions, and practical insights into current trends and challenges in advanced electronic packaging, with a focus on how materials-driven approaches can enhance performance and reliability in modern electronic systems.

TRAINERS PROFILE



Ts Dr Zainal Arif Burhanudin served as an Associate Professor in the Department of Electrical & Electronic Engineering, and now in Department of Applied Sciences at Universiti Teknologi PETRONAS, with over 17 years of research experience in semiconductor electronics and more than 3 years of industry exposure. Holding a PhD in Nanotechnology, he brings a strong combination of academic excellence, practical industry insight, and hands-on research expertise that makes his training sessions highly relevant to professionals in semiconductor industry.

His expertise spans semiconductor devices, nanoelectronics, advanced materials, and electronic packaging technologies, with particular emphasis on semiconductor fabrication processes. His research work includes conductive nanocomposites, carbon nanotube-graphene integration, GaN-based LED technologies, and simulation-driven semiconductor performance optimization, i.e., areas closely aligned with modern advanced packaging challenges such as thermal management, interconnect reliability, heterogeneous integration, and next-generation device performance.

Participants in his training programs benefit from clear technical explanations, industry-relevant case studies, and practical insights into current trends in semiconductor advanced packaging, packaging reliability, process challenges, and future packaging technologies.

RELATED ADVANCED PACKAGING TRAINING COURSES

Upon completion of this beginner-level training, participants may further enhance their knowledge and skills by progressing to the following intermediate-level training programs.

INTERMEDIATE LEVEL

- CoWoS Technology for AI Systems and HPC Packaging Integration (1 day)
- Advanced Packaging Thermal Management for 2.5D and HPC Applications (1 day)
- Advanced Packaging Reliability and Failure Mode (1 day)

TRAINING PROVIDER



ABOUT CREST

Launched in 2012, CREST was formed to address Malaysia's E&E needs to grow the Research, Development and Commercialisation (R&D&C) ecosystem through market driven collaborative R&D and Talent Development. While CREST is industry-led, its member representation is the triple helix of Government, Industry and Academia. As of July 2023, CREST is officially an agency of Ministry of Trade, Investment and Industry (MITI).

ABOUT ETSI

In alignment with the National Semiconductor Strategic Plan (NSS), the development of local talent is a key pillar in driving the growth of the Electrical & Electronics (E&E) industry, with a particular focus on semiconductor technology. To meet the projected industry demand, the NSS targets the training of 60,000 engineers. In support of this objective, the Engineering Talent for Semiconductor Industry (ETSI) program has been established by CREST as a strategic talent development initiative to facilitate the effective implementation of the NSS.

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