

ENGINEERING TALENT FOR SEMICONDUCTOR INDUSTRY PROGRAM

ETS I

CoWoS Technology for AI Systems and HPC Packaging



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INTRODUCTION

This course introduces Chip-on-Wafer-on-Substrate (CoWoS) technology and its role in enabling advanced AI and high-performance computing systems. Participants will learn the fundamentals of CoWoS architecture, fabrication processes, and heterogeneous integration techniques used to combine multiple compute and memory dies into a high-performance package.

COURSE OVERVIEW

The 1-day course covers CoWoS technology variants (CoWoS-S, CoWoS-R, and CoWoS-L), interposer design, die bonding, and 3D stacking with High-Bandwidth Memory (HBM). It also compares CoWoS with competing technologies such as Intel EMIB and Foveros, highlighting differences in performance, scalability, and manufacturing approaches.

In addition, the course examines the advantages, technical challenges, and future directions of advanced packaging technologies. A practical case study on HPC accelerator system optimization provides insight into real-world design trade-offs and integration strategies.

By the end of the course, participants will understand the key concepts, applications, and engineering considerations of CoWoS technology for modern semiconductor systems.

COURSE OUTCOME

Upon successful completion this course, participants will be able to:

- Explain the fundamental concepts, architecture, and evolution of Chip-on-Wafer-on-Substrate (CoWoS) technology in advanced semiconductor packaging.
- Describe the fabrication flow and integration processes involved in CoWoS packaging, including interposer fabrication, die placement, bonding, and substrate integration.
- Differentiate between CoWoS technology variants (CoWoS-S, CoWoS-R, and CoWoS-L) and evaluate their applications in AI and high-performance computing systems.
- Compare CoWoS with competing advanced packaging technologies such as Intel EMIB and Intel Foveros in terms of performance, scalability, and manufacturing considerations.
- Analyze the advantages, challenges, and system-level design trade-offs of CoWoS-based architectures, including 3D stacking, HBM integration, and HPC accelerator optimization.

TARGET PARTICIPANT

This course is designed for technical professionals seeking intermediate-level knowledge of Advanced Packaging.

- Semiconductor process engineers
- Packaging engineers
- Product & test engineers
- R&D engineers in advanced packaging
- Q&R Engineers
- Design Engineers
- Yield Engineers
- Projects leads
- Integration Engineers
- Technical professionals in the field of advanced packaging

Day	Training Outline
<p style="text-align: center;">Day 1 9am - 5pm</p>	<p>1. Introduction to CoWoS Technology</p> <ul style="list-style-type: none"> • Evolution of chip-on-wafer-on-substrate architecture • Key applications in AI and high-performance computing
	<p>2. Concepts</p> <ul style="list-style-type: none"> • Definition of CoWoS • Why was CoWoS developed
	<p>3. Architecture and Fabrication Flow</p> <ul style="list-style-type: none"> • Key components in CoWoS • Interposer fabrication processes • Die placement and bonding • Integration with package substrate
	<p>4. CoWoS Technology Variants</p> <ul style="list-style-type: none"> • CoWoS-S (Silicon Interposer) • CoWoS-R (Redistribution Layer Interposer) • CoWoS-L (Large-Scale Interposer) • CoWoS applications
	<p>5. Comparative Technology Analysis</p> <ul style="list-style-type: none"> • CoWoS vs Intel EMIB • CoWoS vs Intel Foveros • Performance, scalability, and manufacturing considerations
	<p>6. 3D Stacking with CoWoS</p> <ul style="list-style-type: none"> • Memory stacking with HBM • Integration of compute chiplets
	<p>7. Advantages and Challenges of CoWoS</p> <ul style="list-style-type: none"> • Advantages from thermal, size & scalability • Interposer scaling challenges
	<p>8. Future Directions</p> <ul style="list-style-type: none"> • Co-Design methodologies, Direct Liquid Cooling, Smart Thermal Management • EMIB-T (Thermal enhancement), TGV (Through Glass Via), Co-optics
	<p>9. Case Study</p>

TRAINERS PROFILE



Ts. Dr. Syed Muhammad Hafiz is a researcher and technopreneur, specialist in advanced materials and nanoelectronics, focused on translating innovation into scalable industrial solutions. He holds a BSc (Hons) in Physics (2011) and a PhD in Materials Science (2017) from Universiti Malaya. His expertise spans across printed hybrid electronics, nanomaterials synthesis and functionalisation, and semiconductor fabrication, with strong capabilities in nano-ink development, additive manufacturing, and CVD-grown graphene. His work directly supports industry needs in flexible electronics, sensor integration, and cost-effective, sustainable manufacturing.

Dr. Syed has led high-impact applied research programmes, including an RM11.85 million Strategic Research Fund (SRF) project on Printed Hybrid Electronics for Electric and Autonomous Vehicles. He has delivered over 30 publications, filed more than 10 patents, and successfully commercialised nanomaterial-based products. His technologies are supported by recognised certifications, including MySTI, GrapheneVerify, and NanoTrusted, enabling stronger market readiness and industry adoption. His innovation excellence has been recognised internationally, including Grand Prix Award at PHILIPPiNEXT 2025 and Gold Medals at the ITEX 2025. Notably, the innovation of graphene conductive inks and its integration into a Smart Child Car Seat technologies were showcased at World Expo 2025 Osaka, demonstrating global-level recognition.

Actively involved in professional networks such as the IEC Working Group on Wearable Electronic Devices & Technologies (TC/S/14) and IEEE Sensors and Nanotechnology community, Dr. Syed brings both technical depth and industry alignment. His training programmes are outcome-driven, equipping participants with practical insights, real-world case studies, and actionable strategies to accelerate development, improve reliability, and scale advanced electronic solutions from lab to market.

RELATED ADVANCED PACKAGING TRAINING COURSES

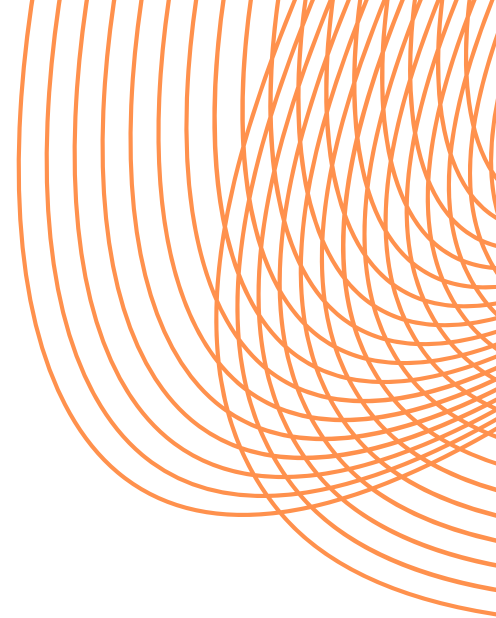
To continue their professional development, participants may progress to the following training programs upon completion of this course.

BEGINNER LEVEL

- Introduction to Advanced Packaging Techniques: 2.5D, 3D, Chiplets and Integration Technologies (2 days)

INTERMEDIATE LEVEL

- Advanced Packaging Thermal Management for 2.5D and HPC Applications (1 day)
- Advanced Packaging Reliability and Failure Mode (1 day)



TRAINING PROVIDER



ABOUT CREST

Launched in 2012, CREST was formed to address Malaysia's E&E needs to grow the Research, Development and Commercialisation (R&D&C) ecosystem through market driven collaborative R&D and Talent Development. While CREST is industry-led, its member representation is the triple helix of Government, Industry and Academia. As of July 2023, CREST is officially an agency of Ministry of Trade, Investment and Industry (MITI).

ABOUT ETSI

In alignment with the National Semiconductor Strategic Plan (NSS), the development of local talent is a key pillar in driving the growth of the Electrical & Electronics (E&E) industry, with a particular focus on semiconductor technology. To meet the projected industry demand, the NSS targets the training of 60,000 engineers. In support of this objective, the Engineering Talent for Semiconductor Industry (ETSI) program has been established by CREST as a strategic talent development initiative to facilitate the effective implementation of the NSS.

CONTACT US

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