CREST
COLLABORATIVE RESEARCH IN ENGINEERING, SCIENCE & TECHNOLOGY

ENGINEERING TALENT FOR SEMICONDUCTOR INDUSTRY PROGRAM

ETSI

Advanced Packaging Reliability and Failure Mode

HRDCORP CLAIMABLE

COLLABORATIVE RESEARCH IN ENGINEERING SCIENCE AND TECHNOLOGY (CREST)
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Advanced Packaging Reliability and Failure Mode

INTRODUCTION

As semiconductor technology transitions from transistor scaling to system-level integration, advanced packaging reliability has become a primary limiter of product performance, yield learning, and field return rate.

COURSE OVERVIEW

Modern advanced packages—such as Fan-Out, 2.5D interposer-based integration, and 3D chiplet architectures—introduce complex material stacks, fine-pitch interconnects, and high power density operation that significantly increase reliability risk This course provides practical, industry-aligned training on advanced packaging reliability and failure modes, focusing on how failures are introduced during design, fabrication, assembly, and packaging, how they interact across multiple domains, and how they are detected, analyzed, and mitigated in real engineering environments.

COURSE OUTCOME

Upon successful completion this course, participants will be able to:

- Explain reliability mechanisms in advanced packaging.
- Identify and classify advanced packaging failure modes.
- Differentiate fab, assembly, and packaging defects.
- Explain multi-physics interaction effects.
- Interpret failure signatures.
- Analyze defect-to-failure progression.
- Apply structured failure analysis methodology
- Evaluate reliability risks at package, board, and system levels.
- Recognize emerging reliability challenges in advanced packaging

TARGET PARTICIPANT

This course is designed for technical professionals seeking intermediate-level knowledge of Advanced Packaging.

- Managers
- Semiconductor process engineers
- Packaging Engineers
- Product & Test Engineers
- R&D Engineers in advanced packaging
- Q&R Engineers
- Design Engineers
- Yield Engineers
- Projects Leads
- Integration Engineers
- Technical professionals in the field of advanced packaging

Day	Training Outline
Day 1 **9am - 5pm**	1. Advanced Packaging Context and Reliability Importance • Evolution from transistor scaling to system-level integration • Role of advanced packaging in AI, High Performance Computing (HPC), mobile, and automotive applications • Reliability as a key limiter of yield and field performance • Design-driven reliability mindset
	2. Reliability Fundamentals for Advanced Packaging • Definition of yield, reliability, and quality • Reliability bathtub curve in advanced packaging context • Infant mortality, useful life, and wear-out mechanisms • Reliability metrics: Failure In Time (FIT) and Mean Time To Failure (MTTF) (conceptual understanding) • Qualification vs characterization vs reliability monitoring • Acceleration concepts: Arrhenius model (temperature dependence) • Fatigue behavior concept (Coffin–Manson relationship) • Electromigration trend concept (Black's equation) • Limitations of standard Joint Electron Device Engineering Council (JEDEC) qualification for advanced packages
	3. Materials, Stress, and Design-for-Reliability (DfR) • Advanced packaging material stack (die, Back End Of Line (BEOL), Redistribution Layer (RDL), solder, substrate) • Coefficient of thermal expansion (CTE) mismatch and mechanical stress • Low-k and ultra-low-k dielectric fragility • Stress sources: thermal, mechanical, electrical, and environmental • Warpage generation and evolution across process flow • Stress transfer from package to die and BEOL • Design-for-Reliability (DfR)
	4. Failure Modes in Advanced Packaging • Solder fatigue • Interconnect Failures • Die and BEOL Failures • Through-Silicon Via (TSV) stress • Package-Level Failures • Advanced Structure Failures • Architecture Comparison

Day	Training Outline
Day 1 9am - 5pm	5.Failure Interaction & Defect Origin Analysis • Thermo-mechanical interaction • Electro-thermal coupling • Moisture interaction • Stress transfer • Fab defects • Assembly defects • Packaging defects
	6.Metrology, Testing, and Reliability Screening • Wafer-level metrology for early reliability risk detection • Package-level inspection: warpage, voids, and delamination • Board-level inspection and solder joint evaluation • Reliability testing: Thermal Cycling Test (TCT), High Temperature Storage Life (HTSL), Temperature Humidity Bias (THB) • X-ray and Scanning Acoustic Microscopy (SAM)
	7.Failure Analysis, Industry Practices & Wrap Up - Electrical vs physical failure correlation - Common failure signatures and interpretation - Misleading signals and incorrect diagnosis risks - Failure analysis strategy and workflow selection
	8.Package, Board, and System-Level Interaction - PCB Coefficient of Thermal Expansion (CTE) mismatch and its impact on package reliability - System stiffness variation (mobile, server, automotive environments) - Influence of heat sink, lid, and thermal interface materials - Board-level vs package-level reliability mismatch - Limitations of JEDEC conditions versus real-world applications
	9. Emerging Reliability Risks and Future Trends - Hybrid bonding reliability challenges - Ultra-fine pitch interconnect (<10 µm) risks - Chiplet interface reliability and heterogeneous integration - High power density effects in AI and HPC systems - Panel-level packaging reliability considerations

TRAINERS PROFILE

Dr. Kamal Nor is a lecturer and researcher in the Department of Mechanical Engineeringat Universiti Teknologi PETRONAS, bringing more than a decade of industry experienceacross manufacturing, reliability and maintenance, and energy generation. He holds aPhD in Mechanical Engineering with a specialization in reliability engineering,combining strong academic credentials with practical industry knowledge and appliedresearch expertise.

His areas of specialization include reliability engineering, modelling, manufacturingprocesses, semiconductor technologies, and engineering materials. His expertiseenables him to address critical challenges in modern semiconductor packaging,particularly in ensuring performance, durability, and process robustness. He brings anintegrated perspective that links material behavior, failure mechanisms, and lifecyclemanagement to real-world packaging reliability and manufacturing demands. Histraining sessions are designed to bridge theory and practice, making them highlyrelevant for beginners to professionals in the semiconductor industry.

Participants in his programs benefit from clear and structured technical delivery, real-world case studies, and actionable insights into current developments in advancedsemiconductor packaging, reliability challenges, process optimization, and emergingpackaging technologies.

RELATED ADVANCED PACKAGING TRAINING COURSES

To continue their professional development, participants may progress to the following training programs upon completion of this course.

BEGINNER LEVEL

- Introduction to Advanced Packaging Techniques: 2.5D, 3D, Chiplets and Integration Technologies (2 days)

INTERMEDIATE LEVEL

- CoWoS Technology for AI Systems and HPC Packaging Integration (1 day)
- Advanced Packaging Thermal Management for 2.5D and HPC Applications (1 day)

TRAINING PROVIDER

ABOUT CREST

Launched in 2012, CREST was formed to address Malaysia's E&E needs to grow the Research, Development and Commercialisation (R&D&C) ecosystem through market driven collaborative R&D and Talent Development. While CREST is industry-led, its member representation is the triple helix of Government, Industry and Academia. As of July 2023, CREST is officially an agency of Ministry of Trade, Investment and Industry (MITI).

ABOUT ETSI

In alignment with the National Semiconductor Strategic Plan (NSS), the development of local talent is a key pillar in driving the growth of the Electrical & Electronics (E&E) industry, with a particular focus on semiconductor technology. To meet the projected industry demand, the NSS targets the training of 60,000 engineers. In support of this objective, the Engineering Talent for Semiconductor Industry (ETSI) program has been established by CREST as a strategic talent development initiative to facilitate the effective implementation of the NSS.

CONTACT US

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