CREST
COLLABORATIVE RESEARCH IN ENGINEERING, SCIENCE & TECHNOLOGY

ENGINEERING TALENT FOR SEMICONDUCTOR INDUSTRY PROGRAM

ETSI

Introduction to Advanced Packaging Techniques: 2.5D, 3D, Chiplets and Integration Technologies

COLLABORATIVE RESEARCH IN ENGINEERING SCIENCE AND TECHNOLOGY (CREST)
https://crest.my/etsi | training@crest.my|04-652 0088

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Introduction to Advanced Packaging Techniques: 2.5D, 3D, Chiplets and Integration Technologies

INTRODUCTION

Step into the world beyond traditional scaling, where innovation is driven not just by silicon, but by how it is integrated. This course offers a compelling introduction to modern semiconductor packaging technologies—focusing on advanced packaging, heterogeneous integration, and chiplet architectures that power today's High-Performance Computing (HPC) and AI systems.

COURSE OVERVIEW

Participants will gain clear insights into how cutting-edge packages are designed and manufactured, exploring key fabrication processes, system-level integration challenges, and reliability considerations. Through real-world industry case studies, the course connects theory to practice—revealing how leading semiconductor companies are pushing performance, bandwidth, and efficiency beyond conventional limits.

By the end of the course, participants will understand how advanced packaging is redefining system architecture and enabling the next generation of computing innovation.

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COURSE OUTCOME

Upon successful completion this course, participants will be able to:

- Describe the fundamentals and evolution of semiconductor packaging technologies.
- Compare traditional and advanced IC packaging methods used in modern electronic systems.
- Explain the principles and processes of 2.5D/3D IC integration and heterogeneous packaging technologies.
- Identify key design, assembly, and reliability challenges in advanced semiconductor packaging.
- Evaluate advanced packaging solutions for applications in AI, HPC, mobile, and data center devices.

TARGET PARTICIPANT

This course is intended for technical professionals who wish to gain foundational knowledge and an introduction to Advanced Packaging.

- Managers
- Semiconductor Process Engineers
- Packaging Engineers
- Product & Test Engineers
- R&D Engineers in advanced packaging
- Q&R Engineers
- Design Engineers
- Yield Engineers
- Projects Leads
- Integration Engineers
- Technical professionals in the field of advanced packaging

Day	Training Outline
Day 1 9am - 5pm (Module 1: Foundations & Overview of IC Packaging Techniques)	1.Fundamentals of Electronic Packaging • Role and functions of semiconductor packaging • Evolution of packaging technologies from wire-bond to advanced packaging • Trends & Key Technologies • Introduction to 3D IC Packaging, 3D IC Integration and 3D Silicon Integration, Yield Introduction • Applications across mobile, High-Performance Computing (HPC), AI, and data center devices
	2.Semiconductor Packaging Structures and Industry Trends • Traditional vs advanced packaging architectures • Industry drivers: Moore's Law limitations and system scaling • Emerging R&D trends in heterogeneous integratio
	3.Overview of Advanced Packaging Technologies • Flip-Chip packaging architecture and assembly • Wafer-Level Packaging (WLP) fundamentals • System-in-Package (SiP) integration approaches
	4.Fan-In and Fan-Out Wafer-Level Packaging • Fan-in Wafer-Level Packaging (WLP) architecture and limitations • Fan-out Wafer-Level Packaging (WLP) process flow and advantages • Panel-level packaging (PLP) developments • Industry case studies of fan-out integration
	5.Workshop/Discussion • Yield case study • Wire bond vs flip chip die area impact

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Day	Training Outline
Day 2 9am - 5pm (Module 2: 3D IC and Heterogeneous Integration)	1.Introduction to 3D IC Concepts and Heterogeneous Integration • Evolution from traditional 2D packaging to 2.5D and 3D IC architectures • Definition and importance of heterogeneous integration in advanced semiconductor systems • Key advantages of 3D integration including higher bandwidth, reduced latency, and improved system performance • Industry applications in AI processors, high-performance computing, and mobile devices
	2.Comparison of Fan-In vs Fan-Out Packages • Overview of Wafer Level Packaging (WLP) technologies • Structure and characteristics of Fan-In Wafer Level Packaging (FIWLP) • Structure and advantages of Fan-Out Wafer Level Packaging (FOWLP) • Comparison of fan-in and fan-out packages in terms of I/O density, package size, and system applications
	3.Overview of Chiplet Technologies, Standards and Design Consideration • Introduction to chiplet-based architecture and system disaggregation • Overview of chiplet interconnect standards such as Universal Chiplet Interconnect Express (UCIe) and Advanced Interface Bus (AIB) • Key design considerations including bandwidth, latency, power delivery, and signal integrity • Benefits of chiplet integration including improved yield, modular
	4.Interposer Technologies • Silicon interposers • Organic interposers • Fabrication techniques and design considerations
	5.Assembly Processes for 2.5D Integration • Die-to-interposer bonding • Microbump assembly • Yield challenges in large interposer systems

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Day	Training Outline
Day 2 9am - 5pm (Module 2: 3D IC and Heterogeneous Integration)	6. Copper-to-Copper and Dielectric Hybrid Bonding • Principles of copper-to-copper direct bonding technology • Overview of dielectric hybrid bonding mechanisms • Key process steps including surface preparation, alignment, bonding, and annealing • Advantages of hybrid bonding for fine pitch interconnect and high-density die stacking
	7.Through Silicon Via (TSV) and Through Glass Via (TGV) Technologies • Introduction to Through Silicon Via (TSV) technology for vertical integration • Key TSV fabrication steps including via etching, insulation, barrier deposition, and copper filling • Overview of Through Glass Via (TGV) technology and glass interposers • Comparison of TSV and TGV in terms of electrical performance, manufacturing complexity, and applications
	8.Microbump Technology and Die Stacking Integration • Introduction to microbump interconnect technology in advanced packaging • Microbump fabrication process including Under Bump Metallurgy (UBM) formation, bump deposition, and reflow • Role of microbumps in 2.5D interposer and 3D IC die stacking • Integration challenges including alignment accuracy, bump pitch scaling, and reliability
	9.Case Study

TRAINERS PROFILE

	Ng Sea Chooi is a master trainer and semiconductor technology specialist with deep expertise in advanced packaging, wafer fabrication processes, and semiconductor manufacturing tools. He develops and delivers high-impact training programs for engineers across all levels, focusing on practical skill-building in areas such as 2.5D/3D integration, fan-out technologies, hybrid bonding, and front-end process fundamentals. In addition to training, Sea Chooi provides consulting support for semiconductor fabrication tools, offering guidance on process setup, equipment capability, and manufacturing best practices. Known for his clarity, technical depth, and hands-on approach, he is committed to elevating engineering competencies within the semiconductor industry.
	Daniel Soon is a semiconductor technology specialist and master trainer with over 20 years of industry experience spanning testing, yield optimization, data analytics, wafer fabrication, and advanced packaging integration, including bumping technology. He develops and delivers high-impact training for both technical and non-technical audiences, translating complex concepts into practical business and operational insights, with focus areas including 2.5D/3D integration, fan-out packaging, and heterogeneous integration. In addition, he provides consulting support in process optimization, yield improvement, and manufacturing best practices, and is known for his clear, structured delivery and ability to bridge engineering knowledge with business understanding.

RELATED ADVANCED PACKAGING TRAINING COURSES

Upon completion of this beginner-level training, participants may further enhance their knowledge and skills by progressing to the following intermediate-level training programs.

INTERMEDIATE LEVEL

- CoWoS Technology for AI Systems and HPC Packaging Integration (1 day)
- Advanced Packaging Thermal Management for 2.5D and HPC Applications (1 day)
- Advanced Packaging Reliability and Failure Mode (1 day)

TRAINING PROVIDER

ABOUT CREST

Launched in 2012, CREST was formed to address Malaysia's E&E needs to grow the Research, Development and Commercialisation (R&D&C) ecosystem through market driven collaborative R&D and Talent Development. While CREST is industry-led, its member representation is the triple helix of Government, Industry and Academia. As of July 2023, CREST is officially an agency of Ministry of Trade, Investment and Industry (MITI).

ABOUT ETSI

In alignment with the National Semiconductor Strategic Plan (NSS), the development of local talent is a key pillar in driving the growth of the Electrical & Electronics (E&E) industry, with a particular focus on semiconductor technology. To meet the projected industry demand, the NSS targets the training of 60,000 engineers. In support of this objective, the Engineering Talent for Semiconductor Industry (ETSI) program has been established by CREST as a strategic talent development initiative to facilitate the effective implementation of the NSS.

CONTACT US

SUFIAN - 012-9480506

sufian@crest.my
training@crest.my