

INOR Lab Tour

Institute Of Nano Optoelectronics Research And Technology (INOR), Universiti Sains Malaysia (USM)

Date: 13 October 2026

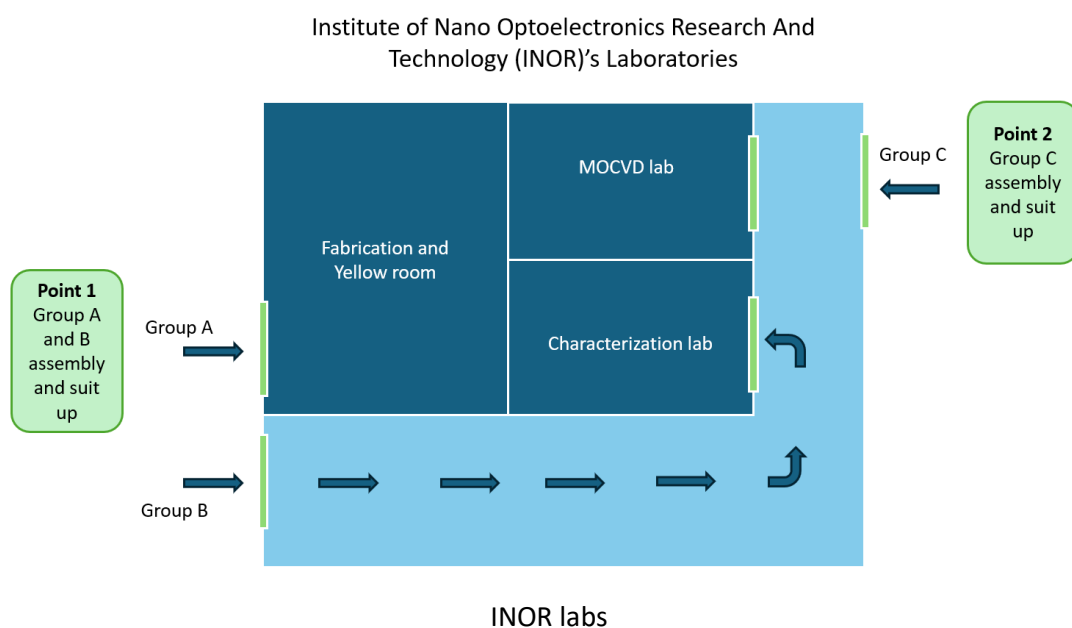
Time: 3.30 PM – 5.00 PM

Venue: INOR, USM SAINS@USM, Block A, Ground Floor, 10, Persiaran Bukit Jambul, Bukit Jambul, 11900 Bayan Lepas, Pulau Pinang

The INOR facility tour at Universiti Sains Malaysia provides a unique opportunity to explore state-of-the-art infrastructure for semiconductor and nanotechnology research. Visitors will experience the full device development workflow, from III-nitride epitaxial growth using MOCVD systems, microfabrication in cleanroom environments, and thin-film processing, to advanced material and device characterization using X-ray diffraction, optical spectroscopy, Hall-effect measurement, and electrical testing platforms. The tour showcases how INOR supports innovation in next-generation electronics, photonics, and power semiconductor technologies.

Tour Flow:

- Assembly Points: Groups A and B will assemble at Point 1 (in front of the INOR office), while Group C will assemble at Point 2 for PPE suiting-up.
- Group Size: Approximately 16-17 participants per group.
- Tour Format: Groups will visit the MOCVD Laboratory, Fabrication & Yellow Room Facilities, and Characterization Laboratory in a rotating schedule.
- Rotation: All groups will begin the tour simultaneously and rotate to the next laboratory every 30 minutes.
- Tour Guides: Tours will be conducted by INOR Lab staff.
- Procedure: Participants will be escorted to their designated laboratory stations and guided throughout the tour.



Layout and Poster Exhibition

Date: 13 October 2026

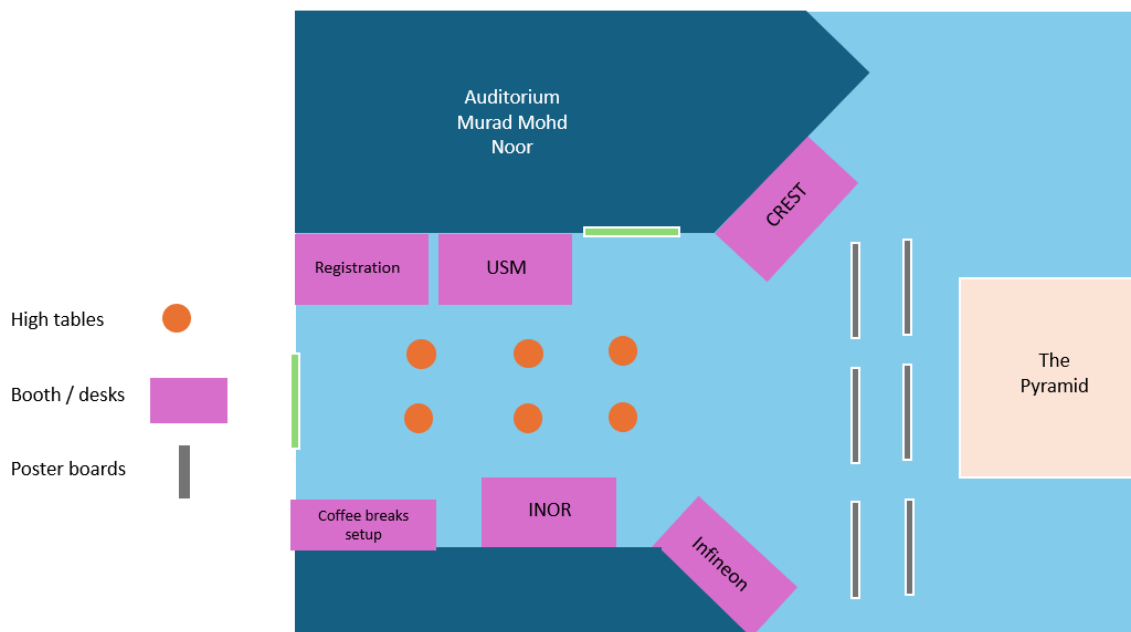
Time: 9.00 AM – 5.00 PM

Venue: Auditorium Murad Mohd Noor, Block C, sains@usm

Theme: High-Voltage Device Physics

An exhibition featuring A1-size posters will be presented by researchers and students from the Institute of Nano Optoelectronics Research and Technology (INOR), Universiti Sains Malaysia (USM), Infineon Technologies, and other participating institutions. The posters will highlight current advances and research activities in the field of High-Voltage Device Physics, showcasing developments in wide-bandgap semiconductor devices, power electronics, device reliability, thermal management, and advanced characterization techniques. The exhibition will be held in front of Auditorium Murad Mohd Noor, Block C, sains@usm, providing participants with opportunities to engage with researchers and explore the latest innovations in next-generation power semiconductor technologies. A total up to 40 posters will be displayed during the exhibition session.

Poster requirements: The poster must be prepared in A1 size (84.1 cm × 59.4 cm) and printed on paper suitable for display. Poster boards will be provided by the organizer, and posters should be ready for pinning onto the designated display boards. The contents should include Title, Introduction, Objectives, Result/Finding, Conclusion.



Layout of Booth Layout and Poster Exhibition

*final layout of arrangements yet to be confirmed