CREST
COLLABORATIVE RESEARCH IN ENGINEERING, SCIENCE & TECHNOLOGY

ENGINEERING TALENT FOR SEMICONDUCTOR INDUSTRY PROGRAM

ETSI

CoWoS Technology for AI Systems and HPC Packaging

HRDCORP CLAIMABLE

COLLABORATIVE RESEARCH IN ENGINEERING SCIENCE AND TECHNOLOGY (CREST)
https://crest.my/etsi | training@crest.my|04-652 0088

CoWoS Technology for AI Systems and HPC Packaging

INTRODUCTION

This course introduces Chip-on-Wafer-on-Substrate (CoWoS) technology and its role in enabling advanced AI and high-performance computing systems. Participants will learn the fundamentals of CoWoS architecture, fabrication processes, and heterogeneous integration techniques used to combine multiple compute and memory dies into a high-performance package.

COURSE OVERVIEW

The 1-day course covers CoWoS technology variants (CoWoS-S, CoWoS-R, and CoWoS-L), interposer design, die bonding, and 3D stacking with High-Bandwidth Memory (HBM). It also compares CoWoS with competing technologies such as Intel EMIB and Foveros, highlighting differences in performance, scalability, and manufacturing approaches.

In addition, the course examines the advantages, technical challenges, and future directions of advanced packaging technologies. A practical case study on HPC accelerator system optimization provides insight into real-world design trade-offs and integration strategies.

By the end of the course, participants will understand the key concepts, applications, and engineering considerations of CoWoS technology for modern semiconductor systems.

COURSE OUTCOME

Upon successful completion this course, participants will be able to:

- Explain the fundamental concepts, architecture, and evolution of Chip-on-Wafer-on-Substrate (CoWoS) technology in advanced semiconductor packaging.
- Describe the fabrication flow and integration processes involved in CoWoS packaging, including interposer fabrication, die placement, bonding, and substrate integration.
- Differentiate between CoWoS technology variants (CoWoS-S, CoWoS-R, and CoWoS-L) and evaluate their applications in AI and high-performance computing systems.
- Compare CoWoS with competing advanced packaging technologies such as Intel EMIB and Intel Foveros in terms of performance, scalability, and manufacturing considerations.
- Analyze the advantages, challenges, and system-level design trade-offs of CoWoS-based architectures, including 3D stacking, HBM integration, and HPC accelerator optimization.

TARGET PARTICIPANT

This course is designed for technical professionals seeking intermediate-level knowledge of Advanced Packaging.

- Semiconductor process engineers
- Packaging engineers
- Product & test engineers
- R&D engineers in advanced packaging
- Q&R Engineers
- Design Engineers
- Yield Engineers
- Projects leads
- Integration Engineers
- Technical professionals in the field of advanced packaging

Day	Training Outline
Day 1 9am - 5pm	1. Introduction to CoWoS Technology • Evolution of chip-on-wafer-on-substrate architecture • Key applications in AI and high-performance computing
	2. Concepts • Definition of CoWoS • Why was CoWoS developed
	3. Architecture and Fabrication Flow • Key components in CoWoS • Interposer fabrication processes • Die placement and bonding • Integration with package substrate
	4. CoWoS Technology Variants • CoWoS-S (Silicon Interposer) • CoWoS-R (Redistribution Layer Interposer) • CoWoS-L (Large-Scale Interposer) • CoWoS applications
	5. Comparative Technology Analysis • CoWoS vs Intel EMIB • CoWoS vs Intel Foveros • Performance, scalability, and manufacturing considerations
	6. 3D Stacking with CoWoS • Memory stacking with HBM • Integration of compute chiplets
	7. Advantages and Challenges of CoWoS • Advantages from thermal, size & scalability • Interposer scaling challenges
	8. Future Directions • Co-Design methodologies, Direct Liquid Cooling, Smart Thermal Management • EMIB-T (Thermal enhancement), TGV (Through Glass Via), Co-optics
	9. Case Study

TRAINERS PROFILE

TJ Yeoh is a seasoned professional with over 30 years of extensive experience in the semiconductor industry, having served with Intel Malaysia in diverse technical and leadership roles. He obtained his Bachelor of Engineering (Mechanical) from University of Canterbury, New Zealand. His expertise spans Assembly and Test Development & Manufacturing, Program & Product Management, Transfers, NPI (New Product Introductions), Strategic Planning and Technical Problem Solving—notably through TRIZ (Theory of Inventive Problem Solving, Level 3) and Model-Based Problem Solving methodologies.

In his most recent role as TSV-R (Through Silicon Via Reveal) Integrator within Intel's Advanced Packaging division, he successfully managed production for the Meteor Lake CPU in the United States, ensuring high-yield integration and manufacturing readiness for next-generation CPU products. TJ is also awarded the certificate for ETSI (Engineering Talent For Semiconductor Industry) Master Trainer Program in Immersive Semiconductor Advance Packaging held in National Tsing Hua University, Taiwan.

Among his key achievements is the global proliferation and adoption of TRIZ (a structured and creative problem solving methodology) across Intel's manufacturing sites in Malaysia, China, Costa Rica, and the Philippines. He has trained over 1,000 engineers, enabling data-driven problem solving and delivering a total ROI exceeding USD 21 million through innovative manufacturing solutions.

RELATED ADVANCED PACKAGING TRAINING COURSES

To continue their professional development, participants may progress to the following training programs upon completion of this course.

BEGINNER LEVEL

- Introduction to Advanced Packaging Techniques: 2.5D, 3D, Chiplets and Integration Technologies (2 days)

INTERMEDIATE LEVEL

- Advanced Packaging Thermal Management for 2.5D and HPC Applications (1 day)
- Advanced Packaging Reliability and Failure Mode (1 day)

TRAINING PROVIDER

ABOUT CREST

Launched in 2012, CREST was formed to address Malaysia's E&E needs to grow the Research, Development and Commercialisation (R&D&C) ecosystem through market driven collaborative R&D and Talent Development. While CREST is industry-led, its member representation is the triple helix of Government, Industry and Academia. As of July 2023, CREST is officially an agency of Ministry of Trade, Investment and Industry (MITI).

ABOUT ETSI

In alignment with the National Semiconductor Strategic Plan (NSS), the development of local talent is a key pillar in driving the growth of the Electrical & Electronics (E&E) industry, with a particular focus on semiconductor technology. To meet the projected industry demand, the NSS targets the training of 60,000 engineers. In support of this objective, the Engineering Talent for Semiconductor Industry (ETSI) program has been established by CREST as a strategic talent development initiative to facilitate the effective implementation of the NSS.

CONTACT US

SUFIAN - 012-9480506

sufian@crest.my
training@crest.my