

ENGINEERING TALENT FOR SEMICONDUCTOR INDUSTRY PROGRAM

ETS I

Advanced Packaging Thermal Management for 2.5D and HPC Applications



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INTRODUCTION

This course provides engineers with a focused understanding of thermal management in advanced semiconductor packaging, with particular emphasis on 2.5D package architectures and high-performance computing (HPC) applications.

As semiconductor devices continue to deliver higher compute density, greater bandwidth, and more compact system integration, thermal management has become a critical design and reliability consideration. In advanced packaging environments, especially for HPC systems, effective heat dissipation and thermal control are essential to maintaining device performance, preventing thermal hotspots, and ensuring long-term package reliability.

COURSE OVERVIEW

Through this course, participants will develop a structured understanding of the thermal fundamentals relevant to advanced packaging, including heat transfer principles, thermal resistance concepts, cooling strategies, hotspot management, package warpage, and reliability concerns under thermal loading. The programme also connects these concepts to practical engineering considerations through real-world industry case discussion involving thermal design approaches for advanced HPC packages.

This course is intended to strengthen participants' technical understanding of how thermal management influences package architecture, cooling solution selection, and system-level performance in modern 2.5D and HPC semiconductor applications..

COURSE OUTCOME

Upon successful completion this course, participants will be able to:

- Explain the role of thermal management in advanced packaging, particularly in 2.5D and HPC semiconductor applications.
- Describe the basic principles of heat transfer, heat flow, and thermal resistance as they relate to package-level thermal behaviour.
- Evaluate major industry cooling strategies used in advanced semiconductor systems, including air cooling, liquid cooling, heat spreaders, heat pipes, vapor chambers, and thermal interface materials.
- Identify key thermal challenges in HPC packages, including high power density, hotspots, thermal runaway risk, and system-level cooling demands.
- Recognize major thermal reliability concerns such as thermal stress, package warpage, and reliability degradation under thermal cycling conditions.
- Relate thermal management concepts to practical engineering challenges through case-based understanding of thermal modelling and cooling optimization in 2.5D package environments.

TARGET PARTICIPANT

This course is designed for technical professionals seeking intermediate-level knowledge of Advanced Packaging.

- Semiconductor Process Engineers
- Packaging Engineers
- Product and Test Engineers
- R&D Engineers in advanced packaging
- Quality and Reliability Engineers
- Design Engineers
- Yield Engineers
- Integration Engineers
- Project or Programme Leads supporting advanced packaging or HPC-related initiatives
- Technical professionals seeking stronger understanding of thermal management challenges in 2.5D and high-performance semiconductor packages

Day	Training Outline
<p style="text-align: center;">Day 1 9am - 5pm</p>	<p>1. Fundamentals of 2.5D Packaging</p> <ul style="list-style-type: none"> • Evolution of semiconductor and chip packaging • Advantage of advance packaging for High-Performance Computing (HPC)
	<p>2. Fundamentals of heat transfer and thermal management</p> <ul style="list-style-type: none"> • Basic heat transfer • Heat flow analysis • Thermal resistance model • Core principle of thermal management
	<p>3. Industry Cooling Strategies</p> <ul style="list-style-type: none"> • Air cooling vs liquid cooling • Heat spreaders, heat pipes and vapor chambers • Thermal Interface Material (TIM) selection • Other cooling strategies (ThermalTSV, Direct Liquid cooling, immerse cooling etc)
	<p>4. Thermal Management in HPC Systems</p> <ul style="list-style-type: none"> • High-Performance Chips Thermal Challenges • Power density of HPC • The Importance of Thermal Management for HPC
	<p>5. Managing Hotspots and Thermal Reliability</p> <ul style="list-style-type: none"> • Managing hot spots and thermal runaway • Thermal stress and package warpage • Reliability concerns under thermal cycling
	<p>6. Case study</p>

TRAINERS PROFILE



Mr. Teoh Lee Chuan is a highly accomplished semiconductor professional with over 25 years of experience in Intel test processes, system integration, and high-volume manufacturing. He holds a Bachelor of Technology with First Class Honors from Universiti Sains Malaysia, combining a strong academic foundation with extensive thermal engineering expertise. His experience includes strategic assignments in Arizona and Oregon, contributing to early development of liquid cooling solutions and thermal interface materials for semiconductor test applications.

His core competencies include New Product Introduction (NPI), yield improvement, and structured problem-solving, complemented by strong leadership in project management. Mr. Teoh has led Intel mechanical system integration teams to develop and manufacture mission-critical testers and thermal modules, ensuring reliability in high-volume production. He is also pioneer participant of the Taiwan ETSI Master Trainer Program in immersive semiconductor advanced packaging, contributing to the development of a future-ready technical workforce.

RELATED ADVANCED PACKAGING TRAINING COURSES

To continue their professional development, participants may progress to the following training programs upon completion of this course.

BEGINNER LEVEL

- Introduction to Advanced Packaging Techniques: 2.5D, 3D, Chiplets and Integration Technologies (2 days)

INTERMEDIATE LEVEL

- CoWoS Technology for AI Systems and HPC Packaging Integration (1 day)
- Advanced Packaging Reliability and Failure Mode (1 day)

TRAINING PROVIDER



ABOUT CREST

Launched in 2012, CREST was formed to address Malaysia's E&E needs to grow the Research, Development and Commercialisation (R&D&C) ecosystem through market driven collaborative R&D and Talent Development. While CREST is industry-led, its member representation is the triple helix of Government, Industry and Academia. As of July 2023, CREST is officially an agency of Ministry of Trade, Investment and Industry (MITI).

ABOUT ETSI

In alignment with the National Semiconductor Strategic Plan (NSS), the development of local talent is a key pillar in driving the growth of the Electrical & Electronics (E&E) industry, with a particular focus on semiconductor technology. To meet the projected industry demand, the NSS targets the training of 60,000 engineers. In support of this objective, the Engineering Talent for Semiconductor Industry (ETSI) program has been established by CREST as a strategic talent development initiative to facilitate the effective implementation of the NSS.

CONTACT US

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